REMARKS

The Office Action mailed March 20, 2001, has been received and reviewed. Claims 1 through 25 are currently pending in the application. Applicant affirms the election to prosecute the invention of group I (claims 1 through 4 and 15 through 25) made during a telephone conversation between Applicant's attorney and the Examiner. Claims 5 through 14 have been withdrawn from consideration as being drawn to a non-elected invention. Claims 1 through 14 and 15 through 25 stand rejected. Applicant has canceled claims 5 through 14, amended claims 1, 2, 4, 15 through 17, 19, 20 and 23, and respectfully requests reconsideration of the application as amended herein.

Claim Objections

Claim 23 stands objected to because of certain writing informalities. Applicant has amended said claim as set forth above to overcome this objection.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,304,737 to Kim

Claims 1 through 4 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kim (U.S. Patent No. 5,304,737). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 of the presently claimed invention is directed to an apparatus for routing interconnections among bond pads on a semiconductor die. As amended herein, the apparatus of claim 1 includes a sheet-like, nonconductive structure having a first surface and a second surface, the second surface being for attachment to the semiconductor die. The apparatus further includes

a plurality of electrically conductive discrete pads which are attached to the first surface of the sheet-like nonconductive structure. The plurality of discrete pads each have an electrical connect portion and a portion facing the first surface of the sheet-like nonconductive structure, with *each discrete pad of the plurality being electrically isolated about its portion facing the first surface of the sheet-like nonconductive structure.* Applicant submits that Kim fails to teach each and every element of claim 1 as amended herein.

Rather, Kim discloses a first pad 12a and a second bond pad 12b, as illustrated in FIG. 5, being electrically connected to an embedded copper foil wiring 12 that is itself connected to a distantly located pad positioned on the opposite end of semiconductor chip 2. This configuration provides a plurality of pads electrically interconnected by way of copper foil wiring 12 via the portions of the bond pads 12a, 12b respectively, facing the first surface. Kim clearly fails to teach an electrically conductive discrete pad being electrically isolated about its portion facing the sheet-like, nonconductive structure. As such, Kim fails to anticipate claim 1 of the presently claimed invention.

Applicant further submits that claims 2 through 4 are not anticipated by Kim based on their dependency from an allowable claim as well as for the independent subject matter introduced thereby.

Further, with respect to claim 2, Kim fails to teach at least one conductor extending between at least two of the electrically conductive discrete pads, the conductor having at least a portion which is external to the sheet-like, nonconductive structure.

Applicant, therefore, submits that claims 1 through 4 are in condition for allowance and respectfully request reconsideration thereof.

Anticipation Rejection Based on U.S. Patent No. 5,905,303 to Kata et al.

Claims 15 through 19 and 21 through 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kata et al. (U.S. Patent No. 5,905,303). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claims 15 and 16

Independent claim 15 is directed to a semiconductor device. The semiconductor device includes a die having a plurality of bond pads disposed on a surface thereof. The device further includes further includes an adapter which has a first plurality of discrete electrical contacts on a first surface of the adapter which are each electrically connected to one the plurality of bond pads. A second plurality of discrete electrical contacts are one a second surface of the adapter with each having an electrical connection portion and a *die facing portion, each of the second plurality being electrically isolated about their die facing portions.* At least some of the second plurality of discrete electrical contacts are in electrical communication with the first plurality of discrete electrical contacts. Additionally, each of the second plurality of discrete electrical contacts have a conductive bump extending therefrom.

In contradistinction, Kata teaches a semiconductor device which includes a die 1, having conductive pads in electrical connection with conductive layers 6. The conductive layers 6 are formed on one surface of an insulating film 3 and are coupled with conductive members 4 which extend through the insulating film. Conductive bumps 9 are in electrical connection with the conductive members 4 adjacent an opposing surface of the insulating film 3. (*See*, col. 4, lies 34-52; FIG. 5). None of the conductive elements (*i.e.*, layers 6, members 4, or bumps 9) have a *die facing portion which is electrically isolated thereabout* as set forth in claim 15. As such, claim 15 of the presently claimed invention is clearly not anticipated by Kata.

Applicant further submits that claim 16 is not anticipated by Kata based on its dependency from an allowable claim as well as for the independent subject matter introduced thereby. Applicant notes that the Office Action mailed on March 20, 2001 rejects claim 16 as being unpatentable under 35 U.S.C. § 102 (b) over Kata et al. but in applying such rejection states that "*Kim* further discloses a protective coating over at least a portion of the die...." (Office Action, page 5, emphasis added). Applicant assumes that the Examiner did not intend to rely on Kim in applying the rejection (it being a § 102 rejection) and that such was simply a typographical error.

Proceeding on the above stated assumption, Applicant traverses the rejection of claim 16 and submits that Kata fails to teach a protective coating over at least a portion of the die with the plurality of conductive bumps be partially exposed through such protective coating.

Applicant, therefore, submits that claims 15 and 16 are in condition for allowance and respectfully requests reconsideration of the same.

Claims 17 through 19 and 21 through 24

Independent claim 17 is directed to a semiconductor device. The semiconductor device includes a die having a plurality of bond pads disposed on a surface thereof. The device further includes an adapter which has a first plurality of discrete electrical contacts on a first surface of the adapter which are each electrically connected to one the plurality of bond pads. A second plurality of discrete electrical contacts are one a second surface of the adapter with each having an electrical connection portion. At least some of the second plurality of discrete electrical contacts are horizontally remote from at least some of the plurality of bond pads disposed on the first surface of the die, the same contact pads being *electrically isolated about their die facing portions*. At least some other of the second plurality of discrete electrical contacts are electrically connected to said first plurality of discrete electrical contacts. Applicant submits that Kata fails to teach each and every element of claim 17 as amended herein

As noted above with respect to the rejection of claims 15 and 16, Kata teaches a semiconductor device which includes a die 1 having conductive pads in electrical connection with conductive layers 6. The conductive layers 6 are formed on one surface of an insulating film 3 and are coupled with conductive members 4 which extend through the insulating film. Conductive bumps 9 are in electrical connection with the conductive members 4 adjacent an opposing surface of the insulating film 3. (*See*, col. 4, lies 34-52; FIG. 5). None of the conductive elements (*i.e.*, layers 6, members 4, or bumps 9) have a *die facing portion which is electrically isolated thereabout* as set forth in claim 17. As such, claim 17 of the presently claimed invention is clearly not anticipated by Kata.

Applicant further submits that claims 18, 19 and 21 through 24 are not anticipated by Kata based on their dependency from an allowable claim as well as for the independent subject matter introduced therein.

Further with respect to claim 18, the Examiner states that "it is inherent to have the thermal coefficient [of] expansion of the chip .... similar to that of the carrier in order to prevent the crack in the device when it operates under high temperatures." (Office Action, page 5). Applicant submits that it is not inherent to have two physically separate components with similar coefficients of thermal expansion. An inherent feature is one which involves the thing's essential character and is based on *intrinsic* properties. The use of two separate and distinct components having similar coefficients of thermal expansion simply can not be regarded as being inherent. Thus, Applicant submits that the subject matter of claim 18 can not be rejected as such.

Further, with respect to claim 19, Applicant notes that the Office Action mailed on March 20, 2001, rejects claim 19 as being unpatentable under 35 U.S.C. § 102 (b) over Kata et al. but in applying such rejection states that "*Kim* further discloses a protective coating over at least a portion of the die...." (Office Action, page 5, emphasis added). Applicant assumes that the Examiner did not intend to rely on Kim in applying the instant rejection (it being a § 102 rejection) and that such was simply a typographical error.

Applicant, therefore, submits that claims 17 through 19 and 21 through 24 are in condition for allowance and respectfully requests reconsideration of the same.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,905,303 to Kata et al. and Further in View of U.S. Patent No. 5,291,062 to Higgins

Claims 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kata et al. (U.S. Patent No. 5,905,303), as applied to claim 19 above, and further in view of Higgins (U.S. Patent No. 5,291,062). Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kata et al. (U.S. Patent No. 5,905,303), as applied to claim 17 above, and further in view of

Higgins (U.S. Patent No. 5,291,062) Applicant respectfully traverses these rejections, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 20 and 25 are improper because the references relied upon by the Examiner fail to teach each and every element set forth in the presently claimed invention.

Claim 20

Claim 20 depends from claim 19 which, in turn, depends from claim 15. Claim 20 recites the additional subject matter of at least one of the second plurality of discrete electrical contacts being electrically isolated from the plurality of bond pads disposed on the first surface of the die. The Examiner cites Higgins as teaching such subject matter and particularly refers to FIG. 6. Applicants respectfully submit that Higgins fails to teach or suggest the subject matter set forth in claim 20.

Higgins teaches an area array semiconductor device having a lid with functional contacts. FIG. 6, which the Examiner particularly relies on, teaches a multichip module formed in a similar manner to the semiconductor devices of FIG. 3. In explaining features of the substrate 104 and the dice 102 of the device shown in FIG. 6, it is stated that "[t]he remaining construction of multichip module 100 is substantially the same as that of the device 10 of FIG. 3." (Col. 8, lines 16-18).

Referring to FIG. 3 and its accompanying description for "the remaining construction," it is noted that a die 12 is electrically connected to traces 18 on a substrate 14 by wire bonds 20. The conductive traces 18 are coupled with mating conductive traces 26 of a lid 22. Plated through-holes 30 formed in the lid 22 electrically couple the mating conductive traces 26 with electrical contact pads 28. "The area array of contact pads 28 uses the entire surface area of the lid, including the area opposing the die 12, for electrical connections which maximizes the density of the contact pads and minimizes the size of the packaged device." (Col. 3, line 40 - col. 4, line 8). The text makes no mention of the contact pads 28 being isolated from the bond pads of the semiconductor die 12.

Furthermore, Applicant submits that FIG. 3 (or corresponding FIG. 6) cannot be relied on as suggesting isolation of some of the contact pads 28 from the bond pads of the semiconductor die 12. FIGS. 3 and 6 (indeed all of the Higgins figures) are cross-sectional views and only disclose certain facets of the disclosed device. Particularly, it is likely that the contact pads 28 in the center portion of the device have plated through-holes 30 which are set back or forward from the plane of the page. This is supported by the specification teaching a maximization of the density of contact pads and a minimization of the package size. Additionally, in conjunction with FIG. 3, Higgins expressly teaches that it "is not necessary that the mating surfaces of traces 18 and 26 be in-line with the plated through-holes 30." Thus, Higgins fails to teach or suggest at least one of the second plurality of discrete electrical contacts being electrically isolated from the plurality of bond pads disposed on the first surface of the die.

Additionally, neither of the references relied upon by the Examiner teach or suggest a plurality of discrete electrical contacts having die facing portions wherein *each of the plurality of contacts are electrically isolated about their die facing portions.*

Applicant submits that claim 20 is clearly allowable over Kata and Higgins, either considered individually or in combination, and respectfully requests reconsideration of the same.

Claim 25

Claim 25, which depends from claim 17, and adds the limitation of having at least one of the second plurality of discrete electrical contacts electrically interconnected with a second die. The Examiner cites Higgins as teaching such subject matter. However, neither Kata nor Higgins teach or suggest a plurality of contacts wherein at least some have *die facing portions which are electrically isolated thereabout*

Applicant submits that claim 25 is clearly allowable over Kata and Higgins, either considered individually or in combination, and respectfully requests reconsideration of the same.

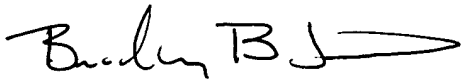
ENTRY OF AMENDMENTS

The amendments to claims 1, 2, 4, 15 through 17, 19, 20 and 23 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1 through 4 and 15 through 25 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully Submitted,



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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the paragraph bridging pages 5 and 6 with the following:

In another preferred embodiment, the jumper pads may be formed over a segment of insulating or dielectric material, such as a [non-conductive] nonconductive film or coating, that is applied to the active surface of the die. The insulating material protects internal circuitry near the active surface from any interference or shorting that may be otherwise generated by the presence of the jumper pad or connections to the jumper pads.

Please replace the paragraph bridging pages 8 and 9 with the following:

In FIGS. 2A and 2B, a semiconductor device 30 having peripheral bond pads 116 includes a sheet-like insulating layer, film or tape segment 32 disposed between an active surface 114 of die 34 and jumper pads 120. The jumper pads 120 are thus formed in or on the tape 32 and the tape 32 is adhesively attached to the active surface [14] 114 of a die 34. The tape 32 may be an adhesive-type tape or bear a thermosetting adhesive 33, one preferred tape being a polyimide film as sold under the trademark Kapton®, or other suitable tapes, tape-like films or sheet structures adhesively attached to active surface 114 using adhesive techniques known in the art. Preferably, the tape 32 is [non-conductive,] nonconductive and thus insulates the active surface 114 of the die 34 from electrical signals that may be passed through the jumper pads 120. The thickness of tape 32 has been exaggerated for clarity but may, in fact, be extremely thin, only of sufficient structural integrity to maintain its form during handling and application to the die.

Please replace the paragraph bridging pages 9 and 10 with the following:

FIG. 3 illustrates yet another preferred embodiment of a semiconductor device 40 according to the present invention in which an adapter 46 converts a peripherally bond padded semiconductor die 42 to a device 40 bearing jumper pads 220. The semiconductor die 42

includes bond pads 216 which have been "bumped;" that is, balls or bumps 44 of gold, solder or conductive adhesive have been attached thereto. An adapter 46 configured to mate with the active surface 214 and bond pads 216 of the die 42 is comprised of a support structure 48, which may be formed of a sheet-like structure, such as Kapton® or other tape as used in tape automated bonding, or a more rigid structure formed from ceramic, silicon, FR-4 or other materials known in the art. Preferably, the adapter 46 is formed from a material having a coefficient of thermal expansion (CTE) substantially matching the CTE of the die 42. The adapter 46 includes a plurality of first contact pads 50 on a top surface 52 thereof and a plurality of second contact pads 54 proximate a bottom surface 56 thereof. The first contact pads 50 are electrically connected to the second contact pads [52] 54 by conductive contacts or vias 58 that extend to and between the first and second contact pads 50 and [52] 54, respectively, and are contained within the support structure 48. The second contact pads 54 are arranged to match the arrangement of bumped bond pads 216. Thus, when the adapter 46 and die 42 are brought together and mutually secured by adhesive 57, the second contact pads 54 mate with the bumped pads 216. As further illustrated in FIG. 3A, the assembled semiconductor device 40 may be dipped or coated with a protective layer 59 of, for example, epoxy or silicon gel to protect and insulate the adapter 46 and the die 42, and the first contact pads 50 may be bumped so that the conductive bumps 61 extend above the protective layer 59 for flip-chip connection to a carrier substrate. In such an arrangement, short conductive traces formed on the carrier substrate would extend between jumper pads 220 and first contact pads 50 to be connected, between a series of jumper pads 220, between a contact pad 50 and an external circuit trace, etc. Alternatively, and as more fully described with respect to FIG. 6, rerouting circuitry may be carried within adapter 46 to reroute a bond pad 216 to a new location of a contact pad 50. It is also an option to employ adapter 46 only as an interposer substrate to provide for flip-chip connection of die 42 to a carrier substrate, omitting jumper pads 220 or any sort of bond pad rerouting capability.

Please replace the paragraph bridging pages 10 and 11 with the following:

As illustrated, wire bonds 80, 81, 82, 83 and 84 can be formed: between bond pad 316 and lead finger 66; between adjacent or proximate bond pads 316; between[,] adjacent or proximate jumper pads 320; between bond pad 316 and jumper pad 320; or between jumper pad 320 and lead finger 66. The termination points of wire bonds 80, 81, 82, 83 and 84 can be of ball, wedge, or other configuration as is known in the art, and formed with a conventional wire bonding machine. Accordingly, a large number of I/O alternative configurations can be achieved for any semiconductor device, depending on the number and layout of jumper pads 320 and configuration of wire bonds.

IN THE CLAIMS

1. (Amended) An apparatus for routing interconnections among bond pads on a semiconductor die, comprising:

a sheet-like, [non-conductive] nonconductive structure having a first surface, and a second surface for attachment to [a] said semiconductor die; and

a plurality of electrically conductive discrete pads attached to said first surface, the plurality of electrically conductive discrete pads each having an electrical connect portion and a portion facing said first surface, each electrically discrete pad of the plurality being electrically isolated about said portion facing said first surface [from the second surface].

2. (Amended) The apparatus of claim 1, further comprising at least one conductor extending between at least two of said plurality of electrically conductive discrete pads, said at least one conductor including at least a portion external to said sheet-like nonconductive structure.

4. (Amended) The apparatus of claim 1, wherein said [non-conductive] nonconductive structure is comprised of a dielectric film or sheet.

15. (Amended) A semiconductor device, comprising:

a die including a plurality of bond pads disposed on a surface thereof;

an adapter having a first plurality of discrete electrical contacts on a first surface thereof, each electrically connected to one of said plurality of bond pads, and [said adapter having] a second plurality of discrete electrical contacts on a second surface thereof, each of said second plurality of discrete electrical contacts having an electrical connection portion and a die facing portion and each being electrically isolated about said die facing portions, at least some of said second plurality of discrete electrical contacts in electrical communication with said first plurality of discrete electrical contacts; and

a plurality of conductive bumps, each extending from one of said second plurality of discrete electrical contacts.

16. (Amended) The semiconductor device of claim 15, further comprising a protective coating over at least a portion of said die, [and with] said plurality of conductive bumps being at least partially exposed through said protective coating.

17. (Amended) A semiconductor device, comprising:

a die including a plurality of bond pads disposed on a first surface thereof;

an adapter having a first plurality of discrete electrical contacts on a first surface thereof, each electrically connected to one of said plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, at least some of said second plurality of discrete electrical contacts being horizontally remote from at least some of the plurality of bond pads disposed on the first surface of the die, the at least some of said second plurality of discrete electrical contacts being electrically isolated about a die facing portion thereof, and at least some other of said second plurality of discrete electrical contacts being electrically connected to said first plurality of discrete electrical contacts [horizontally offset therefrom through conductors carried by said adapter].

19. (Amended) The semiconductor device of claim 15, wherein the adapter comprises at least one conductive via extending between at least one of the first plurality of discrete electrical contacts and at least one of the at least some other of said second plurality of discrete electrical contacts.

20. (Amended) The semiconductor device of claim 19, wherein at least [some] one of the second plurality of discrete electrical contacts [are] is electrically isolated from the plurality of bond pads disposed on the first surface of the die.

23. (Amended) The semiconductor device of claim 17, further comprising a plurality of conductive vias extending through said adapter electrically connecting said first plurality of discrete electrical contacts and the at least some other of the second plurality of discrete electrical contacts [wherein at least one of the conductors carried by the adapter are internal to the adaptor].